19-2424; Rev 2; 5/06

Ultra-Low Offset/Drift, Low-Noise, Precision SOT23 Amplifiers

MAX4238/MAX4239

General Description

The MAX4238/MAX4239 are low-noise, low-drift, ultra-high precision amplifiers that offer near-zero DC offset and drift through the use of patented autocorrelating zeroing techniques. This method constantly measures and compensates the input offset, eliminating drift over time and temperature and the effect of 1/f noise. Both devices feature rail-to-rail outputs, operate from a single 2.7V to 5.5V supply, and consume only 600µA. An active-low shutdown mode decreases supply current to 0.1µA.

The MAX4238 is unity-gain stable with a gain-bandwidth product of 1MHz, while the decompensated MAX4239 is stable with $A_V \geq 10V/V$ and a GBWP of 6.5MHz. The MAX4238/MAX4239 are available in 8-pin narrow SO, 6-pin TDFN and SOT23 packages.

Applications

Thermocouples

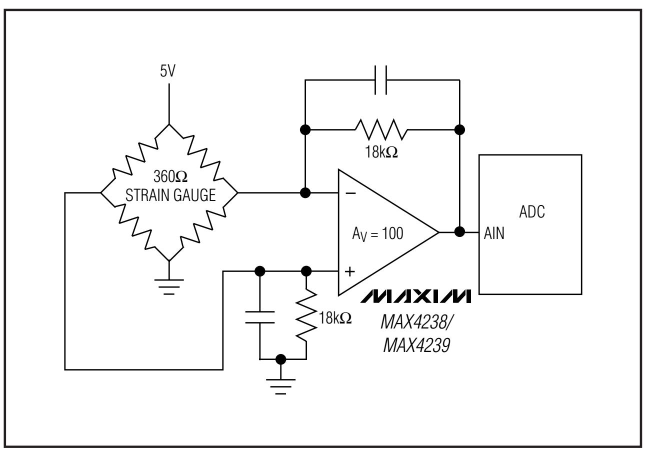
Strain Gauges

Electronic Scales

Medical Instrumentation

Instrumentation Amplifiers

Typical Application Circuit



Features

- ♦ **Ultra-Low, 0.1µV Offset Voltage**
  - **2.0µV (max) at +25°C**
  - **2.5µV (max) at -40°C to +85°C**
  - **3.5µV (max) at -40°C to +125°C**
- ♦ **Low 10nV/°C Drift**
- ♦ **Specified over the -40°C to +125°C Automotive Temperature Range**
- ♦ **Low Noise: 1.5µV_{P-P} from DC to 10Hz**
- ♦ **150dB A_{VOL}, 140dB PSRR, 140dB CMRR**
- ♦ **High Gain-Bandwidth Product**
  - **1MHz (MAX4238)**
  - **6.5MHz (MAX4239)**
- ♦ **0.1µA Shutdown Mode**
- ♦ **Rail-to-Rail Output (R_L = 1kΩ)**
- ♦ **Low 600µA Supply Current**
- ♦ **Ground-Sensing Input**
- ♦ **Single 2.7V to 5.5V Supply Voltage Range**
- ♦ **Available in a Space-Saving 6-Pin SOT23 and TDFN Packages**

Ordering Information

PART	PIN-PACKAGE	TOP MARK	PKG CODE
MAX4238AUT-T	6 SOT23-6	AAZZ	U6F-6
MAX4238ASA	8 SO	—	S8-4
MAX4238ATT+T	6 TDFN-EP*	+ANG	T633-2
MAX4239AUT-T	6 SOT23-6	ABAA	U6F-6
MAX4239ASA	8 SO	—	S8-4
MAX4239ATT+T	6 TDFN-EP*	+ANH	T633-2

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

+Denotes lead-free package.

**EP = Exposed paddle.*

Selector Guide

PART	MINIMUM STABLE GAIN	GAIN BANDWIDTH (MHz)
MAX4238	1V/V	1
MAX4239	10V/V	6.5

Pin Configurations appear at end of data sheet.

Ultra-Low Offset/Drift, Low-Noise, Precision SOT23 Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC} to GND)..6V
All Other Pins ....(GND - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration
(OUT shorted to V_{CC} or GND) ....Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin Plastic SOT23
(derate 9.1mW/°C above +70°C) 727mW
8-Pin Plastic SO (derate 5.88mW/°C above +70°C).....471mW
6-Pin TDFN-EP (derate 18.2mW above +70°C).........1454mW
Operating Temperature Range ....-40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range..............................-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(2.7V ≤ V_{CC} ≤ 5.5V, V_{CM} = GND = 0V, V_{OUT} = V_{CC}/2, R_L = 10kΩ connected to V_{CC}/2, $\overline{SHDN}$ = V_{CC}, **T_A = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)			0.1	2	µV
Long-Term Offset Drift					50		nV/1000hr
Input Bias Current	I_B	(Note 2)			1		pA
Input Offset Current	I_{OS}	(Note 2)			2		pA
Peak-to-Peak Input Noise Voltage	e_{nP-P}	R_S = 100Ω, 0.01Hz to 10Hz			1.5		$µV_{P-P}$
Input Voltage-Noise Density	e_n	f = 1kHz			30		nV/√Hz
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test		GND - 0.1		V_{CC} - 1.3	V
Common-Mode Rejection Ratio	CMRR	-0.1V ≤ V_{CM} ≤ V_{CC} - 1.3V (Note 1)		120	140		dB
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{CC} ≤ 5.5V (Note 1)		120	140		dB
Large-Signal Voltage Gain	A_{VOL}	0.05V ≤ V_{OUT} ≤ V_{CC} - 0.05V (Note 1)	R_L = 10kΩ	125	150		dB
		0.1V ≤ V_{OUT} ≤ V_{CC} - 0.1V (Note 1)	R_L = 1kΩ	125	145		
Output Voltage Swing	V_{OH}/V_{OL}	R_L = 10kΩ	V_{CC} - V_{OH}		4	10	mV
			V_{OL}		4	10	
		R_L = 1kΩ	V_{CC} - V_{OH}		35	50	
			V_{OL}		35	50	
Output Short-Circuit Current		To either supply			40		mA
Output Leakage Current		0 ≤ V_{OUT} ≤ V_{CC}, $\overline{SHDN}$ = GND (Note 2)			0.01	1	µA
Slew Rate		V_{CC} = 5V, C_L = 100pF, V_{OUT} = 2V step	MAX4238		0.35		V/µs
			MAX4239		1.6		
Gain-Bandwidth Product	GBWP	R_L = 10kΩ, C_L = 100pF, measured at f = 100kHz	MAX4238		1		MHz
			MAX4239		6.5		
Minimum Stable Closed-Loop Gain		R_L = 10kΩ, C_L = 100pF, phase margin = 60°	MAX4238		1		V/V
			MAX4239		10		

ELECTRICAL CHARACTERISTICS (continued)

($2.7V \le V_{CC} \le 5.5V$, V_{CM} = GND = 0V, $V_{OUT} = V_{CC}/2$, $R_L = 10k\Omega$ connected to $V_{CC}/2$, $\overline{SHDN} = V_{CC}$, **T_A = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Closed-Loop Gain		$R_L = 10k\Omega$, C_L = 100pF, phase margin = 60°	MAX4238		1000		V/V
			MAX4239		6700		
Settling Time		-1V step	0.1% (10 bit)		0.5		ms
			0.025% (12 bit)		1.0		
			0.006% (14 bit)		1.7		
			0.0015% (16 bit)		2.3		
Overload Recovery Time		A_V = 10 (Note 4)	0.1% (10 bit)		3.3		ms
			0.025% (12 bit)		4.1		
			0.006% (14 bit)		4.9		
			0.0015% (16 bit)		5.7		
Startup Time		A_V = 10	0.1% (10 bit)		1.8		ms
			0.025% (12 bit)		2.6		
			0.006% (14 bit)		3.4		
			0.0015% (16 bit)		4.3		
Supply Voltage Range	V_{CC}	Inferred by PSRR test		2.7		5.5	V
Supply Current	I_{CC}	$\overline{SHDN} = V_{CC}$, no load, V_{CC} = 5.5V			600	850	µA
		$\overline{SHDN}$ = GND, V_{CC} = 5.5V			0.1	1	
Shutdown Logic-High	V_{IH}			2.2			V
Shutdown Logic-Low	V_{IL}					0.8	V
Shutdown Input Current		$0V \le V_{\overline{SHDN}} \le V_{CC}$			0.1	1	µA

ELECTRICAL CHARACTERISTICS

($2.7V \le V_{CC} \le 5.5V$, V_{CM} = GND = 0V, $V_{OUT} = V_{CC}/2$, $R_L = 10k\Omega$ connected to $V_{CC}/2$, $\overline{SHDN} = V_{CC}$, **T_A = -40°C to +125°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	T_A = -40°C to +85°C			2.5	µV
			T_A = -40°C to +125°C			3.5	
Input Offset Drift	TCV_{OS}	(Note 1)			10		nV/°C
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test		GND - 0.05		V_{CC} - 1.4	V
Common-Mode Rejection Ratio	CMRR	GND - 0.05V ≤ $V_{CM} \le V_{CC}$ - 1.4V (Note 1)	T_A = -40°C to +85°C	115			dB
			T_A = -40°C to +125°C	90			
Power-Supply Rejection Ratio	PSRR	$2.7V \le V_{CC} \le 5.5V$ (Note 1)		120			dB
Large-Signal Voltage Gain	A_{VOL}	$R_L = 10k\Omega$, $0.1V \le V_{OUT} \le V_{CC} - 0.1V$ (Note 1)	T_A = -40°C to +85°C	125			dB
			T_A = -40°C to +125°C	95			
		$R_L = 1k\Omega$ (Note 1)	$0.1V \le V_{OUT} \le V_{CC} - 0.1V$, T_A = -40°C to +85°C	120			dB
			$0.2V \le V_{OUT} \le V_{CC} - 0.2V$, T_A = -40°C to +125°C	80			
Output Voltage Swing	V_{OH}/V_{OL}	$R_L = 10k\Omega$	$V_{CC} - V_{OH}$			20	mV
			V_{OL}			20	
		$R_L = 1k\Omega$	$V_{CC} - V_{OH}$			100	
			V_{OL}			100	
Output Leakage Current		$0V \le V_{OUT} \le V_{CC}$, $\overline{SHDN}$ = GND (Note 3)				2	µA
Supply Voltage Range	V_{CC}	Inferred by PSRR test		2.7		5.5	V
Supply Current	I_{CC}	$\overline{SHDN} = V_{CC}$, no load, V_{CC} = 5.5V				900	µA
		$\overline{SHDN}$ = GND, V_{CC} = 5.5V				2	
Shutdown Logic High	V_{IH}			2.2			V
Shutdown Logic Low	V_{IL}					0.7	V
Shutdown Input Current		$0V \le V_{\overline{SHDN}} \le V_{CC}$				2	µA

Note 1: Guaranteed by design. Thermocouple and leakage effects preclude measurement of this parameter during production testing. Devices are screened during production testing to eliminate defective units.

Note 2: IN+ and IN- are gates to CMOS transistors with typical input bias current of 1pA. CMOS leakage is so small that it is impractical to test and guarantee in production. Devices are screened during production testing to eliminate defective units.

Note 3: Leakage does not include leakage through feedback resistors.

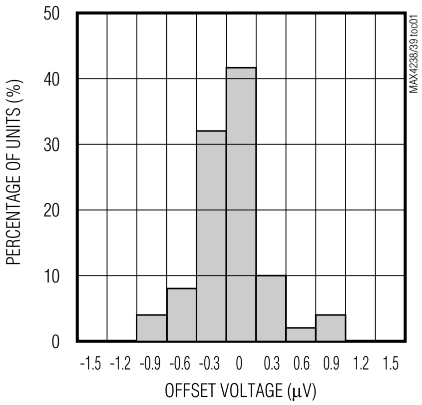
Note 4: Overload recovery time is the time required for the device to recover from saturation when the output has been driven to either rail.

Note 5: Specifications are 100% tested at T_A = +25°C, unless otherwise noted. Limits over temperature are guaranteed by design.

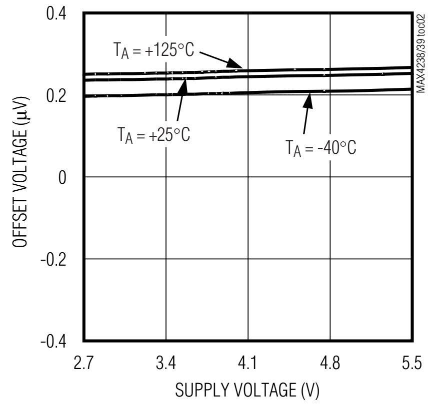
Typical Operating Characteristics

(V_{CC} = 5V, V_{CM} = 0V, R_L = 10kΩ connected to V_{CC}/2, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

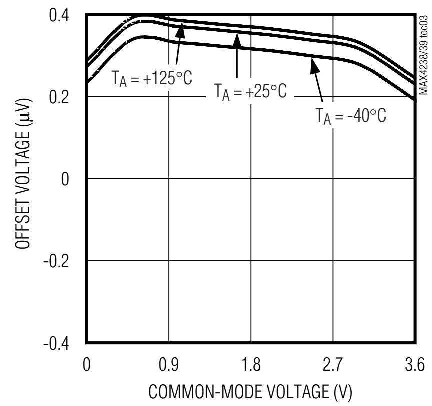
INPUT OFFSET DISTRIBUTION



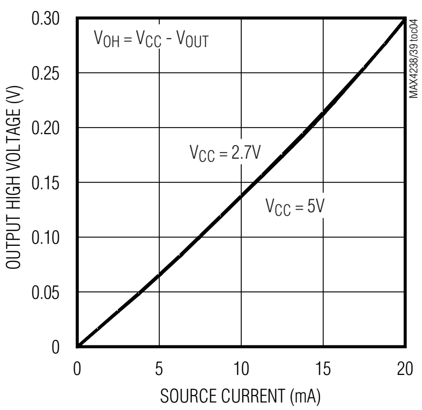
OFFSET VOLTAGE vs. SUPPLY VOLTAGE



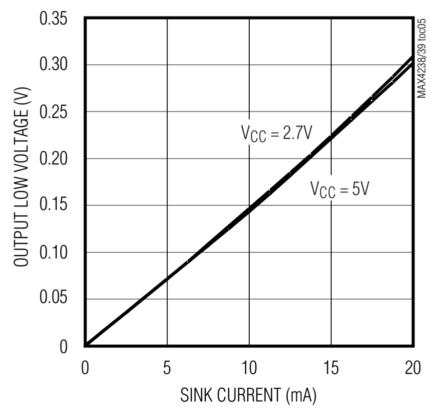
OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



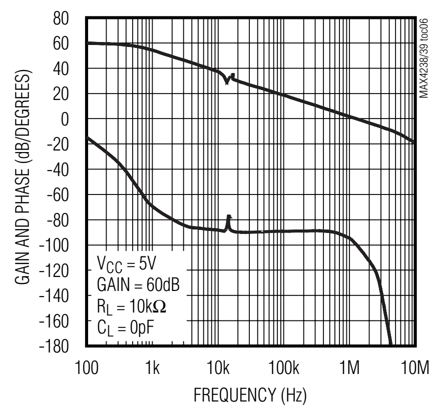
OUTPUT HIGH VOLTAGE vs. OUTPUT SOURCE CURRENT



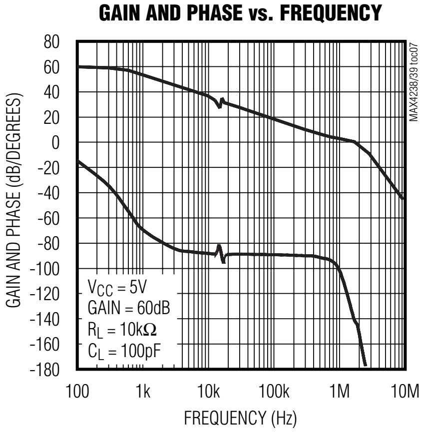
OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



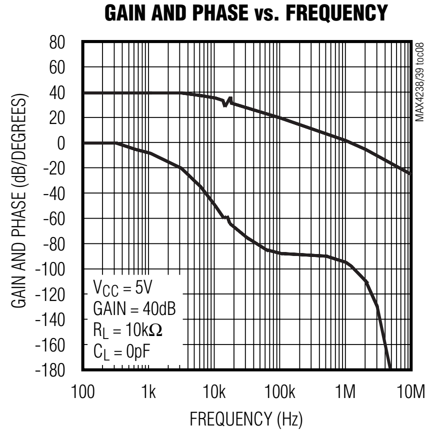
MAX4238 GAIN AND PHASE vs. FREQUENCY



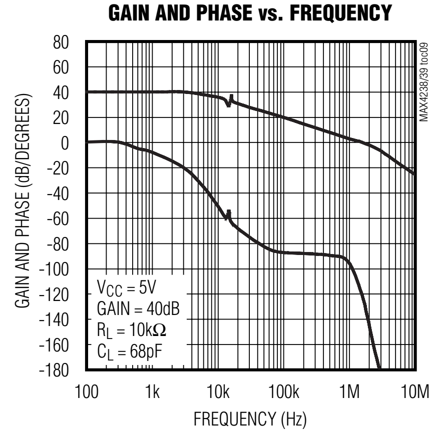
MAX4238 GAIN AND PHASE vs. FREQUENCY



MAX4238 GAIN AND PHASE vs. FREQUENCY



MAX4238 GAIN AND PHASE vs. FREQUENCY

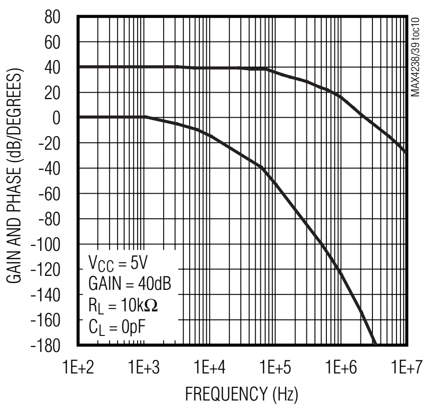


Ultra-Low Offset/Drift, Low-Noise, Precision SOT23 Amplifiers

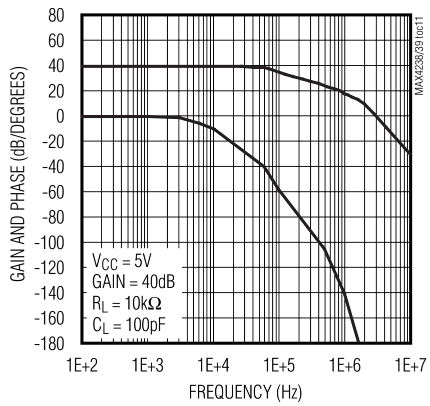
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CM} = 0V, R_L = 10kΩ connected to $V_{CC}/2$, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

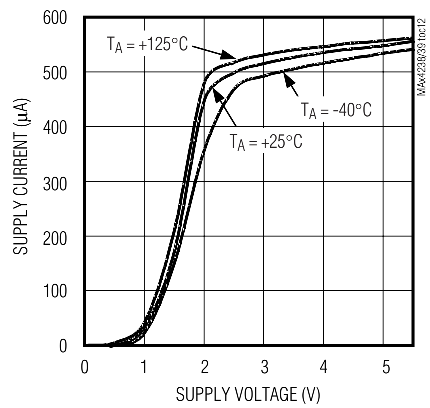
MAX4239
GAIN AND PHASE vs. FREQUENCY



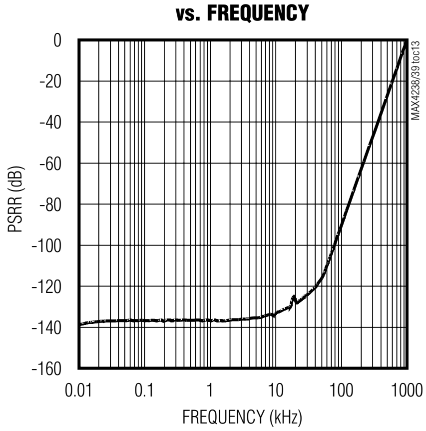
MAX4239
GAIN AND PHASE vs. FREQUENCY



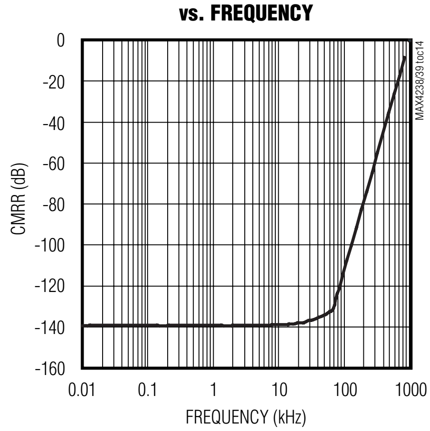
SUPPLY CURRENT vs. SUPPLY VOLTAGE



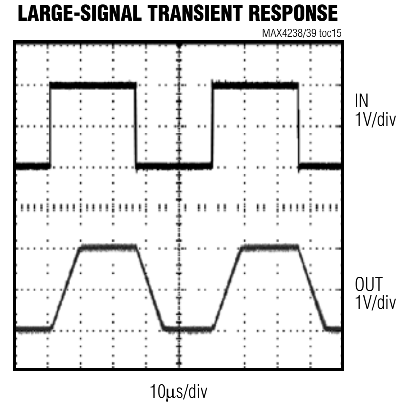
POWER-SUPPLY REJECTION RATIO
vs. FREQUENCY



COMMON-MODE REJECTION RATIO
vs. FREQUENCY

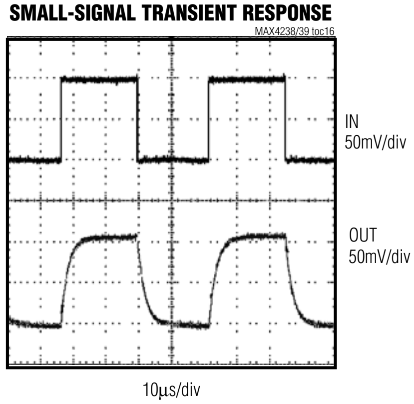


MAX4238
LARGE-SIGNAL TRANSIENT RESPONSE



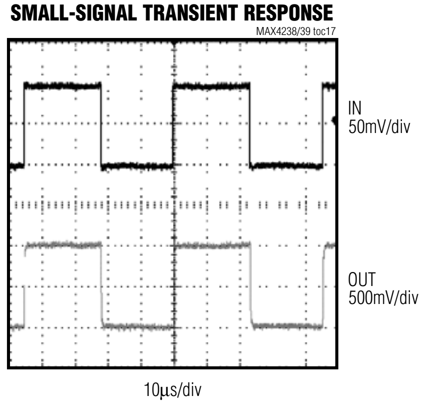
A_V = 1V/V
R_L = 2kΩ
C_L = 100pF

MAX4238
SMALL-SIGNAL TRANSIENT RESPONSE



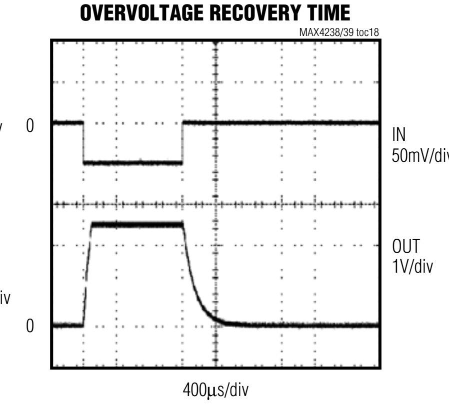
A_V = 1V/V
R_L = 2kΩ
C_L = 100pF

MAX4239
SMALL-SIGNAL TRANSIENT RESPONSE



A_V = 10V/V
R_L = 2kΩ
C_L = 100pF

OVERVOLTAGE RECOVERY TIME

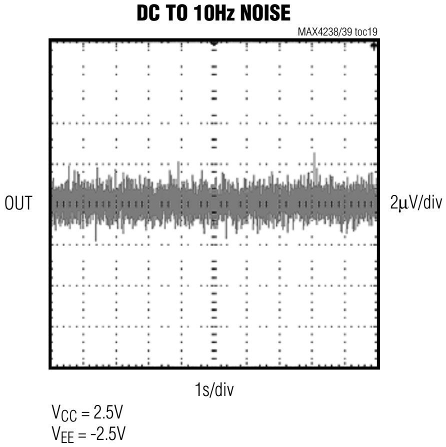


A_V = 100V/V
R_L = 10kΩ
V_{CC} = 2.5V
V_{EE} = -2.5V

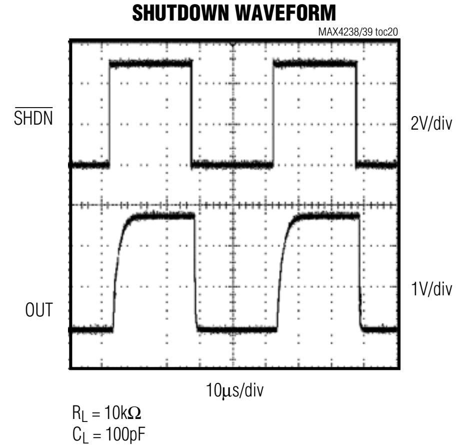
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CM} = 0V, R_L = 10kΩ connected to $V_{CC}/2$, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

DC TO 10Hz NOISE



SHUTDOWN WAVEFORM



Pin Description

PIN			NAME	FUNCTION
TDFN	SOT23	SO		
1	1	6	OUT	Amplifier Output
2	2	4	GND	Ground
3	3	3	IN+	Noninverting Input
4	4	2	IN-	Inverting Input
5	5	1	$\overline{SHDN}$	Shutdown Input. Active-low shutdown, connect to V_{CC} for normal operation.
6	6	7	V_{CC}	Positive Power Supply
—	—	5, 8	N.C.	No Connection. Not internally connected.
EP	—	—	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX4238/MAX4239 are high-precision amplifiers that have less than 2.5µV of input-referred offset and low 1/f noise. These characteristics are achieved through a patented autozeroing technique that samples and cancels the input offset and noise of the amplifier. The pseudorandom clock frequency varies from 10kHz to 15kHz, reducing intermodulation distortion present in chopper-stabilized amplifiers.

Offset Error Sources

To achieve very low offset, several sources of error common to autozero-type amplifiers need to be considered. The first contributor is the settling of the sampling capacitor. This type of error is independent of input-source impedance, or the size of the external gain-setting resistors. Maxim uses a patented design technique to avoid large changes in the voltage on the sampling capacitor to reduce settling time errors.

The second error contributor, which is present in both autozero and chopper-type amplifiers, is the charge injection from the switches. The charge injection appears as current spikes at the input, and combined with the impedance seen at the amplifier's input, contributes to input offset voltage. Minimize this feedthrough by reducing the size of the gain-setting resistors and the input-source impedance. A capacitor in parallel with the feedback resistor reduces the amount of clock feedthrough to the output by limiting the closed-loop bandwidth of the device.

The design of the MAX4238/MAX4239 minimizes the effects of settling and charge injection to allow specification of an input offset voltage of 0.1µV (typ) and less than 2.5µV over temperature (-40°C to +85°C).

1/f Noise

1/f noise, inherent in all semiconductor devices, is inversely proportional to frequency. 1/f noise increases 3dB/octave and dominates amplifier noise at lower frequencies. This noise appears as a constantly changing voltage in series with any signal being measured. The MAX4238/MAX4239 treat 1/f noise as a slow varying offset error, inherently canceling the 1/f noise.

Ultra-Low Offset/Drift, Low-Noise, Precision SOT23 Amplifiers

Output Overload Recovery

Autozeroing amplifiers typically require a substantial amount of time to recover from an output overload. This is due to the time it takes for the null amplifier to correct the main amplifier to a valid output. The MAX4238/MAX4239 require only 3.3ms to recover from an output overload (see *Electrical Characteristics* and *Typical Operating Characteristics*).

Shutdown

The MAX4238/MAX4239 feature a low-power (0.1µA) shutdown mode. When $\overline{SHDN}$ is pulled low, the clock stops and the device output enters a high-impedance state. Connect $\overline{SHDN}$ to V_{CC} for normal operation.

Applications Information

Minimum and Maximum Gain Configurations

The MAX4238 is a unity-gain stable amplifier with a gain-bandwidth product (GBWP) of 1MHz. The MAX4239 is decompensated for a GBWP of 6.5MHz and is stable with a gain of 10V/V. Unlike conventional operational amplifiers, the MAX4238/MAX4239 have a maximum gain specification. To maintain stability, set the gain of the MAX4238 between A_V = 1000V/V to 1V/V, and set the gain of the MAX4239 between A_V = 6700V/V and 10V/V.

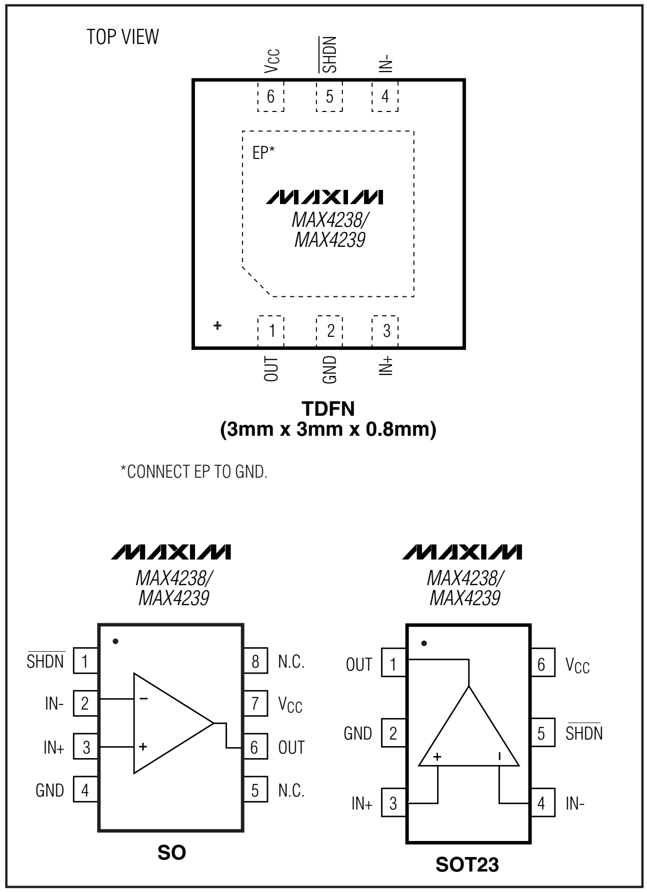
ADC Buffer Amplifier

The low offset, fast settling time, and 1/f noise cancellation of the MAX4238/MAX4239 make these devices ideal for ADC buffers. The MAX4238/MAX4239 are well suited for low-speed, high-accuracy applications such as strain gauges (see *Typical Application Circuit*).

Error Budget Example

When using the MAX4238/MAX4239 as an ADC buffer, the temperature drift should be taken into account when determining the maximum input signal. With a typical offset drift of 10nV/°C, the drift over a 10°C range is 100nV. Setting this equal to 1/2LSB in a 16-bit system yields a full-scale range of 13mV. With a single 2.7V supply, an acceptable closed-loop gain is A_V = 200. This provides sufficient gain while maintaining headroom.

Pin Configurations



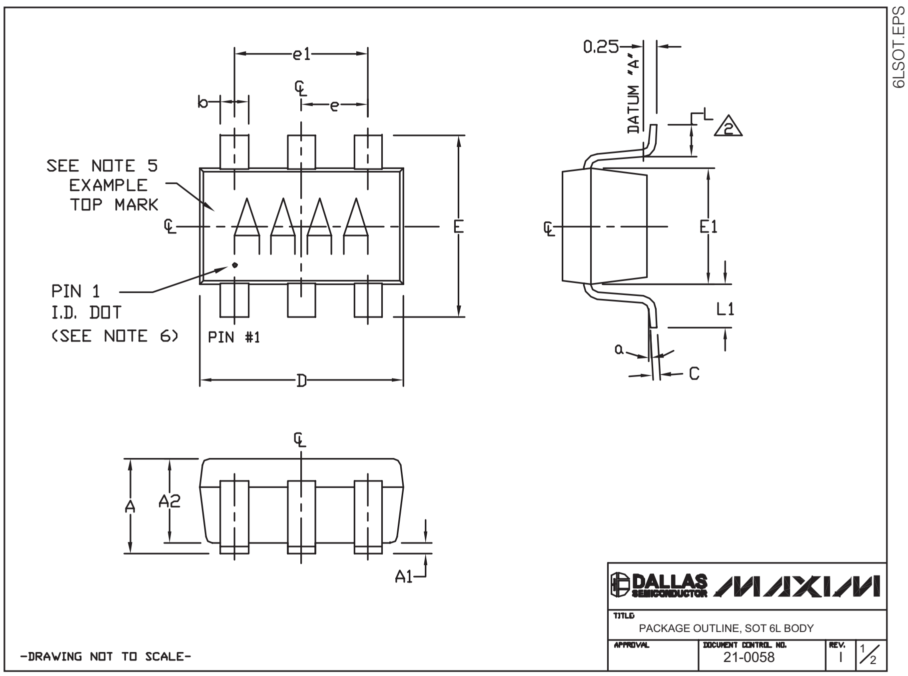
Chip Information

TRANSISTOR COUNT: 821

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3mm ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF.		
e1	1.90 BSC.		
e	0.95 BSC.		
α	0°	2.5°	10°

PKG CODES:
U6-1, U6-2, U6-4, U6C-8, U6SN-1, U6CN-2, U6S-3, U6F-5, U6F-6, U6FH-5, U6FH-6

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT 6L BODY

APPROVAL | DOCUMENT CONTROL NO. 21-0058 | REV. I | 2/2

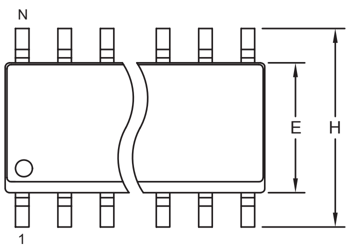
-DRAWING NOT TO SCALE-

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

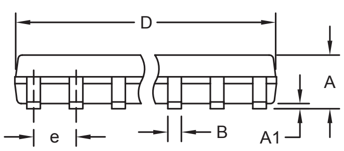
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



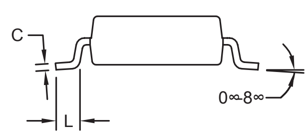
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

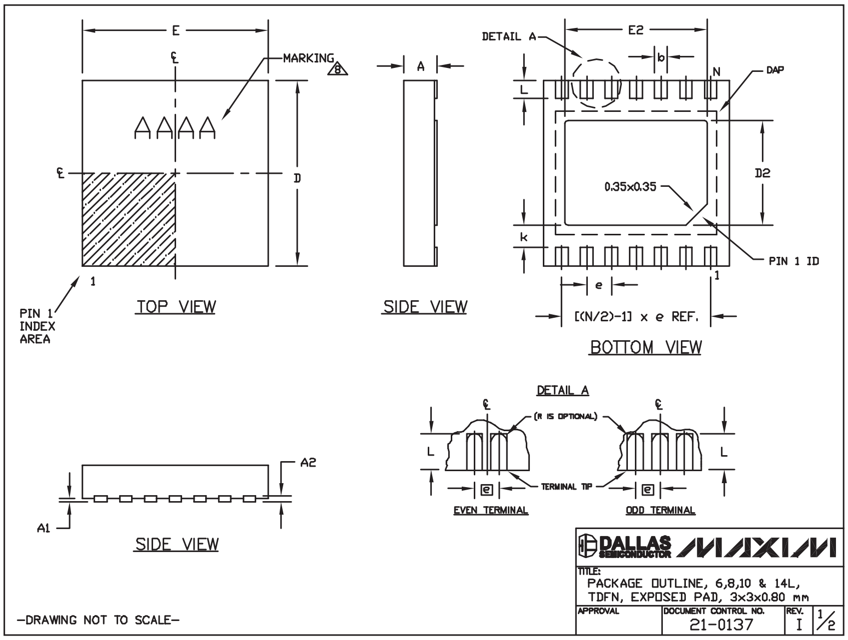
TITLE:

PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0137 | REV. I | 2/2

MAX4238/MAX4239 Package Code: T633-2

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